AMENDMENTS TO THE SPECIFICATION

Please replace paragraph [0002] with the following amended paragraph:

This application is related to co-pending U.S. Patent Applications No. 10/632,226 and No. 10/632,219 ~~entitled APPARATUS AND METHOD FOR EFFICIENTLY UPDATING BRANCH TARGET ADDRESS CACHE (docket cntr.2140) and APPARATUS AND METHOD FOR RESOLVING DEADLOCK FETCH CONDITIONS INVOLVING BRANCH TARGET ADDRESS CACHE (docket cntr.2144) and~~ filed concurrently herewith.

Please delete the section entitled "SUMMARY OF THE INVENTION" in its entirety and substitute the following section therefor:

SUMMARY OF THE INVENTION

The present invention provides a method and apparatus for invalidating redundant entries in a BTAC for the same branch instruction, thereby avoiding wasting space in the BTAC with the redundant entries. In one aspect the present invention provides an apparatus in a pipelined microprocessor for invalidating a redundant entry for the same branch instruction in a set associative branch target address cache (BTAC). The apparatus includes a way specifier, generated in a first pipeline stage, for specifying one of a plurality of ways of the BTAC for storing a target address of a branch instruction present in a cache line specified by an instruction cache fetch address missing in the BTAC. The apparatus also includes a request, generated in a second pipeline stage, for requesting the BTAC to write a resolved target address of the branch instruction into the one of the plurality of ways specified by the way specifier in the first pipeline stage. The second pipeline stage is subsequent to the first pipeline stage and the first and second pipeline stages are separated by at least three pipeline stages. The apparatus also includes a status indicator, for indicating whether at least two ways of a set of the BTAC selected by an instruction cache fetch address contain a valid branch target address for a same branch instruction. The apparatus also includes control logic, coupled to the status indicator, for invalidating one of the at least two ways of the selected set if the status indicator indicates

at least two ways of the selected set contain a valid branch target address for a same branch instruction.

In another aspect, the present invention provides an apparatus in a pipelined microprocessor for invalidating redundant entries for the same branch instruction in a branch target address cache (BTAC). The apparatus includes a way specifier, generated in a first pipeline stage, for specifying one of a plurality of ways of the BTAC for storing a target address of a branch instruction present in a cache line specified by an instruction cache fetch address missing in the BTAC. The apparatus also includes a request, generated in a second pipeline stage, for requesting the BTAC to write a resolved target address of the branch instruction into the one of the plurality of ways specified by the way specifier in the first pipeline stage. The second pipeline stage is subsequent to the first pipeline stage and the first and second pipeline stages are separated by at least three pipeline stages. The apparatus also includes detection logic, for detecting a condition in which more than one valid way of a plurality of ways of a selected set of the BTAC are storing a target address for a same branch instruction. The apparatus also includes invalidation logic, coupled to the detection logic, for invalidating all but one of the more than one valid way of the selected set.

In another aspect, the present invention provides a pipelined microprocessor. The microprocessor includes an instruction cache, having an address input for receiving an address to select a line including a branch instruction. The microprocessor also includes a branch target address cache (BTAC), coupled to the instruction cache, for generating a plurality of indicators in response to the address. Each of the plurality of indicators indicates whether a corresponding way in a set of the BTAC selected by the address is storing a valid target address of the branch instruction. The microprocessor also includes logic, coupled to the BTAC, configured to invalidate one or more of the plurality of ways of the selected set if the plurality of indicators indicates two or more of the plurality of ways is storing a valid target address of the branch instruction. The microprocessor also includes a first pipeline stage, in which the BTAC indicates a miss of the address therein, and in which the BTAC specifies one of the plurality of ways for storing the target address. The microprocessor also includes a second pipeline stage, subsequent to the first

pipeline stage, which requests the BTAC to write a resolved target address of the branch instruction into the one of the plurality of ways specified by the BTAC in the first pipeline stage. The first and second pipeline stages are separated by at least three pipeline stages.

In another aspect, the present invention provides a method for invalidating redundant entries in a set-associative branch target address cache (BTAC) for the same branch instruction. The method includes determining whether a tag of more than one way of a set of the BTAC selected by an index portion of an instruction cache fetch address matches a tag portion of the instruction cache fetch address and is valid. The method also includes invalidating all but one way of the selected set, if more than one way of the selected set is valid and matching. The method also includes indicating, in a first pipeline stage, a miss of the address in the BTAC and specifying one of the plurality of ways for storing a target address of a branch instruction included in a cache line selected by the address in an instruction cache. The method also includes requesting the BTAC, in a second pipeline stage, to write a resolved target address of the branch instruction into the one of the plurality of ways specified by the BTAC in the first pipeline stage, wherein the second pipeline stage is subsequent to the first pipeline stage and the first and second pipeline stages are separated by at least three pipeline stages.

In another aspect, the present invention provides a method for invalidating a redundant entry for the same branch instruction in the same set of an N-way set associative branch target address cache (BTAC). The method includes selecting an N-way set in the BTAC with a lower portion of an instruction fetch address. The method also includes comparing N address tags of N corresponding ways of the N-way set with an upper portion of the instruction fetch address. The method also includes determining whether two or more of the N address tags match the upper portion and are valid. The method also includes invalidating, if two or more of the N address tags match the upper portion and are valid, one or more of the N ways corresponding to the two or more of the valid N address tags matching the upper portion. The method also includes indicating, in a first pipeline stage, a miss of the address in the BTAC and specifying one of the N ways for storing a target address of a branch instruction included in a cache line selected by the address in an

instruction cache. The method also includes requesting the BTAC, in a second pipeline stage, to write a resolved target address of the branch instruction into the one of the N ways specified by the BTAC in the first pipeline stage, wherein the second pipeline stage is subsequent to the first pipeline stage and the first and second pipeline stages are separated by at least three pipeline stages.

In another aspect, the present invention provides a computer program embodied on a computer-readable medium, comprising computer-readable program code for providing a pipeline microprocessor. The program code includes first program code for providing an instruction cache, having an address input for receiving an address to select a line including a branch instruction. The program code also includes second program code for providing a branch target address cache (BTAC), coupled to the instruction cache, for generating a plurality of indicators in response to the address. Each of the plurality of indicators indicates whether a corresponding way in a set of the BTAC selected by the address is storing a valid target address of the branch instruction. The program code also includes third program code for providing logic, coupled to the BTAC, configured to invalidate one or more of the plurality of ways of the selected set if the plurality of indicators indicates two or more of the plurality of ways is storing a valid target address of the branch instruction. The program code also includes fourth program code for providing a first pipeline stage, in which the BTAC indicates a miss of the address therein, and in which the BTAC specifies one of the plurality of ways for storing the target address. The program code also includes fifth program code for providing a second pipeline stage, subsequent to the first pipeline stage, which requests the BTAC to write a resolved target address of the branch instruction into the one of the plurality of ways specified by the BTAC in the first pipeline stage. The first and second pipeline stages are separated by at least three pipeline stages.

An advantage of the present invention is that it potentially improves the efficiency of a BTAC by enabling target addresses to be cached for a greater number of branch instructions by eliminating redundant target addresses for the same branch instruction.

Other features and advantages of the present invention will become apparent upon study of the remaining portions of the specification and drawings.